

CLAIMS

Having thus described out invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method for fabricating a silicon-on-insulator (SOI) substrate comprising the steps of:

(a) subjecting a Si-containing substrate to a base oxygen ion implantation step to create a first structure having a damaged implant region within the Si-containing substrate;

(b) subjecting the first structure to a room temperature oxygen ion implantation step to create a second structure having an amorphized implant region adjacent to said damaged implanted region; and

(c) performing an annealing process on said second structure, wherein at least one of steps (a)-(c) is performed under conditions that are capable of providing an SOI substrate comprising a buried oxide having a breakdown field of greater than 5 MV/cm, with the proviso that when step (a) is selected to achieve said breakdown field the base oxygen ion implantation step is performed using an oxygen ion dose of about $2.5 \times 10^{17} \text{ cm}^{-2}$ or less, when step (b) is selected to achieve said breakdown field the room temperature oxygen implant step is performed at an energy that is about 5 to about 20 % less than an energy used during the base oxygen ion implantation step, or when step (c) is selected to achieve said breakdown field a pre-annealing soak cycle is employed prior to an internal oxidation step.

2. The method of Claim 1 wherein steps (b) and (c) are selected to achieve said breakdown field.

3. The method of Claim 1 wherein steps (a)-(c) are selected to achieve said breakdown field.
4. The method of Claim 1 wherein step (c) is selected to achieve said breakdown field.
5. The method of Claim 1 further comprising providing a patterned masking material or dielectric cap to said Si-containing substrate prior to performing step (a).
6. The method of Claim 5 wherein said patterned masking material or dielectric cap is removed after performing step (b) or after performing step (c).
7. The method of Claim 1 wherein the base oxygen ion implantation step is performed utilizing a single ion implantation step or multiple ion implantation steps.
8. The method of Claim 1 wherein the room temperature oxygen ion implantation step is performed utilizing a single ion implantation step or multiple ion implantation steps.
9. The method of Claim 1 wherein annealing process comprises a ramp-up anneal, an internal oxidation, annealing and a ramp-down step.
10. The method of Claim 1 wherein said annealing process forms a surface oxide on said Si-containing substrate.
11. The method of Claim 10 further comprising a step of removing said surface oxide from said Si-containing substrate by planarization or selective etching.
12. The method of Claim 1 wherein step (a) is selected to achieve said breakdown field and said oxygen ion dose is from about 2.0×10^{17} to about $2.4 \times 10^{17} \text{ cm}^{-2}$.

13. The method of Claim 1 wherein step (a) is performed in an ion beam apparatus that operates at a beam current from about 1 to about 100 milliamps and an energy from about 1 to about 10,000 keV.

14. The method of Claim 1 wherein step (a) is performed at a substrate temperature from about 100° to about 800°C.

15. The method of Claim 1 wherein step (b) is selected to achieve said breakdown field and said energy is off-set to a value from about 6 to about 8 % lower than the energy of said base oxygen ion implantation step.

16. The method of Claim 1 wherein step (b) is selected to achieve said breakdown field and said energy is from about 155 to about 165 keV.

17. The method of Claim 1 wherein step (b) is performed using an oxygen ion dose from about $1E15$ to about $5E15\text{ cm}^{-2}$.

18. The method of Claim 1 wherein step (b) is performed at a temperature from about 1 Kelvin to about 200°C.

19. The method of Claim 1 wherein step (c) is selected to achieve said breakdown field and said annealing process includes a ramp-up step, said pre-annealing soak, said internal oxidation annealing, annealing and a cool-down step.

20. The method of Claim 19 wherein said pre-annealing soak is performed at a temperature of about 1250°C or greater.

21. The method of Claim 19 wherein said pre-annealing soak is performed for a time period from about 5 minutes to about 5 hours.

22. The method of Claim 19 wherein said ramp-up step, said pre-annealing soak, said annealing and said cool-down step are performed in the same or different ambient that comprises an inert gas containing less than 10% oxygen.

23. The method of Claim 19 wherein said pre-annealing soak is performed in an ambient containing greater than 30 % oxygen.

24. A method of fabricating a silicon-on-insulator substrate (SOI) comprising the steps of:

(a) subjecting a Si-containing substrate to a base oxygen ion implantation step to create a first structure having a damaged implant region within the Si-containing substrate;

(b) subjecting the first structure to a room temperature oxygen ion implantation step to create a second structure having an amorphized implant region adjacent to said damaged implanted region, wherein said room temperature oxygen implant step is performed at an energy that is about 5 to about 20 % less than an energy used during the base oxygen ion implantation step; and

(c) performing an annealing process on said second structure, wherein an SOI substrate is provided that comprises a buried oxide having a breakdown field of greater than 5 MV/cm.

25. A method for fabricating a silicon-on-insulator (SOI) substrate comprising the steps of:

(a) subjecting a Si-containing substrate to a base oxygen ion implantation step to create a first structure having a damaged implant region within the Si-containing substrate;

(b) subjecting the first structure to a room temperature oxygen ion implantation step to create a second structure having an amorphized implant region adjacent to said damaged implanted region; and

(c) performing an annealing process on said second structure, said annealing process includes a pre-annealing soak cycle employed prior to an internal oxidation step, wherein an SOI substrate is provided that comprises a buried oxide having a breakdown field of greater than 5 MV/cm.

26. A method for fabricating a silicon-on-insulator substrate comprising the steps of: ✓

(a) subjecting a Si-containing substrate to a base oxygen ion implantation step to create a first structure having a damaged implant region within the Si-containing substrate;

(b) subjecting the first structure to a room temperature oxygen ion implantation step to create a second structure having an amorphized implant region adjacent to said damaged implanted region, said room temperature oxygen ion implantation step is performed at an energy that is about 5 to about 20 % less than an energy used during the base oxygen ion implantation step; and

(c) performing an annealing process on said second structure, said annealing process includes a pre-annealing soak cycle employed prior to an internal oxidation step, wherein an SOI substrate is provided comprises a buried oxide having a breakdown field of greater than 5 MV/cm.

27. A method for fabricating a silicon-on-insulator substrate comprising the steps of: ✓

(a) subjecting a Si-containing substrate to a base oxygen ion implantation step to create a first structure having a damaged implant region within the Si-containing substrate, said

base oxygen ion implantation step is performed using an ion dose of about 2.5 cm^{-2} or less at an energy of 170 keV or greater;

(b) subjecting the first structure to a room temperature oxygen ion implantation step to create a second structure having an amorphized implant region adjacent to said damaged implanted region, said room temperature oxygen ion implantation step is performed at an energy that is about 5 to about 20 % less than an energy used during the base oxygen ion implantation step; and

(c) performing an annealing process on said second structure, said annealing process includes a pre-annealing soak cycle employed prior to an internal oxidation step, wherein an SOI substrate is provided comprises a buried oxide having a breakdown field of greater than 5 MV/cm.